terminal, the interposer having at least one electrically conductive interconnect electrically coupling the at least one bond pad of the semiconductor die positioned adjacent to the die attach surface to the at least external terminal positioned adjacent to the external surface, the interposer being formed of an organic substrate or a polyimide substrate; and

H1 cont.

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges and disposed between the semiconductor die and the interposer, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges of the semiconductor die, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.

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amd 14

H2

N. (Four Times Amended) A device package assembly for a semiconductor die being constructed from a process comprising:

laminating a plurality of strips of compliant adhesive film to an interposer having at least one electrically conductive interconnect, the interposer being formed of an organic substrate or a polyimide substrate and further having a die attach surface to which the semiconductor die is attached, and an external surface opposite of the die attach surface;

attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges, the strips of compliant adhesive film having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first

adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die; and

bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad.

38. (Three Times Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.

42. (Four Times Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which at least one electrically conductive bond pad is fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die to adhere the carrier layer to the die attach surface of the interposer, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips of compliant adhesive film further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.

H4 Cont.

REMARKS

Claims 1-3, 5-15, 17, 18, 38-45 and 50-53 are pending in the application as of the Office Action dated September 11, 2002. However, claims 5, 6, 7, 17 and 39 were cancelled in the Amendment dated July 25, 2002, which has been acknowledged and made of record by Examiner Berezny. Therefore, claims 1-3, 8-15, 18, 38, 40-45 and 50-53 are currently pending in the application. In the Office Action dated September 11, 2002, the Examiner rejected claims 1-3, 8-15, 18, 38, 40-45 and 50-53 under U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,169,328 to Mitchell ("Mitchell") in view of U.S. Patent No. 5,461,255 to Chan *et al.* ("Chan"). Applicant disagrees with this ground of rejection and wishes to clarify various distinctions of Applicant's invention over the cited art. Reconsideration of the application is therefore requested in view of the present amendment and following remarks.

In the Advisory Action dated November 18, 2002, the Examiner noted that an Examiner Amendment agreed to by the undersigned during a telephonic interview occurring on